Abstract

A clock and data recovery unit for recovering a received serial data bit stream having phase adjustment means for adjustment of a sampling time in the center of a unit interval (UI) of the received data bit stream, wherein the phase adjustment means comprises means for generating equidistant reference phase signals; a phase interpolation unit (PIU) which rotates the generated reference phase signals with a predetermined granularity in response to a rotation control signal; an oversampling unit (OSU) for oversampling the received data stream with the rotated reference phase signals according to a predetermined oversampling rate (OSR); a serial-to-parallel-conversion unit which converts the oversampled data stream into a deserialized data stream with a predetermined decimation factor (DF); a binary phase detection unit (BPD) for detecting an average phase difference (AVG-PH) between the received serial data bit stream and the rotated reference phase signal by adjusting a phase detector gain (PDG) depending on the actual data density (DD) of the deserialized data stream such that the variation of the average phase detection gain (PDG) is minimized; and a loop filter for filtering the detected average phase difference (AVG-PH) to generate the rotation control signal for the phase interpolation unit (PIU); data recognition means (DRM) for recovery of the received data stream which includes a number of parallel data recognition FIR-Filters, wherein each data recognition FIR-Filter comprises a weighting unit for weighting data samples of the deserialized data stream around the sampling time adjusted by the phase adjustment means; a summing unit for summing up the weighted data samples; and a comparator unit for comparing the summed up data samples with a threshold value to detect the logic value of a data bit within the received serial data bit stream.

Fig. 7